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TITLE: METHOD FOR ELECTROPLATING AND CONTACT PROJECTION ARRANGEMENT

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METHOD FOR ELECTROPLATING AND CONTACT PROJECTION ARRANGEMENT

PRIORITY CLAIM

[0001] The present application is a continuation of International Patent Application Serial No. PCT/EP2004/052999, filed November 17, 2004, and claims the benefit of priority of German Patent Application No. 103 55 953.1, filed November 29, 2003, both of which are hereby incorporated by reference.

BACKGROUND

[0002] 1. Technical Field

[0003] The invention relates to a method of electroplating. In particular, the invention relates to a method of electroplating for a contact projection.

[0004] 2. Background Information

[0005] Copper is a very inexpensive material having a high electrical conductivity. Consequently, a copper layer is well suited to supplying the current during electroplating. Therefore, copper is a material that is often used as a material for the auxiliary layer.

[0006] The mask layer is e.g. a resist layer which is patterned by means of a photolithographic method. For example, a contact projection made of a solderable material, which is also referred to in the jargon as "soldering bump", is electrodeposited in the mask opening. Tin alloys, for example, in particular tin-lead alloys or more environmentally compatible tin-silver alloys, are used as soldering material.

[0007] The basic layer, the auxiliary layer and the mask layer are preferably applied over the whole area. The basic layer and the auxiliary layer are applied by sputtering, for example.

[0008] During electroplating, the substrate to be coated is dipped into an electrolyte bath and connected as cathode. On account of the electrochemical processes brought about by the voltage, material - the so-called cations - deposits from the electrolyte on the substrate. Optional additives in the electrolyte bath

enable specific properties of the deposited layer to be influenced in a targeted manner.

BRIEF SUMMARY

[0009] The invention relates to a method for electroplating in which the following steps are performed:

[0010] application of an electrically conductive basic layer to a substrate,

[0011] application of an auxiliary layer having better electrical conductivity in comparison with the basic layer after the application of the basic layer,

[0012] application of a mask layer after the application of the auxiliary layer, e.g. a resist layer,

[0013] production of a mask with at least one mask opening from the mask layer, electroplating of a layer in the mask opening.

[0014] The substrate is for example a semiconductor substrate with one metallization layer or with a plurality of metallization layers. Silicon semiconductor substrates are often used. The metallization contains for example more than eighty atomic percent of aluminum or more than eighty atomic percent of copper.

[0015] The electrically conductive basic layer is e.g. an adhesion promoting layer for increasing the mechanical adhesion and/or a diffusion barrier layer for preventing diffusion. By way of example, titanium nitride layers are used as copper barrier layers. In connection with a contact projection, the basic layer and auxiliary layer are also referred to in the jargon as "under bump metallization" (UBM).

[0016] It is an object of the invention to specify an improved method for electroplating which can be used in particular to produce contact projections having good mechanical and electrical properties. Moreover, the intention is to specify a contact projection having good mechanical and electrical properties.

[0017] The object referring to the method is achieved by means of a method having the method steps specified in patent claim 1. Developments are specified in the subclaims.

[0018] In the case of the method according to the invention, in addition to the method steps mentioned in the introduction, the following steps are performed:

[0019] patterning of the auxiliary layer using the mask or resist mask, the basic layer not being patterned or not being completely patterned according to the resist mask, and

[0020] electroplating of a layer in the resist opening after the patterning of the auxiliary layer.

[0021] The invention is based on the consideration that the auxiliary layer is on the one hand required for rapid electroplating with homogeneous layer growth. On the other hand, residues of the auxiliary layer below the deposited layer are often disturbing, for example with regard to corrosion or with regard to the formation of specific interfaces. Therefore, the auxiliary layer is removed in the case of the method according to the invention by means of a mask beneath a resist opening, said mask being required anyway for the definition of the electroplating zone. In this case, however, the basic layer is not concomitantly removed beneath the resist opening. The basic layer is likewise electrically conductive and thus suitable for current transport during electroplating.

[0022] The lower current-carrying capacity of the basic layer is not of very great consequence since the auxiliary layer is present as far as the mask opening and is used for current transport. In the comparatively small electroplating zone in comparison with the substrate surface, the current-carrying capacity is increased as the thickness of the deposited layer increases. By way of example, the electroplating zone has an area of less than 40 percent or less than 20 percent of the substrate surface.

[0023] New layer sequences can be electrodeposited by the method according to the invention because restrictions are circumvented by the auxiliary layer. It is thus possible to produce in particular contact projections having good electrical properties, in particular having high resistance to electromigration, and having a high mechanical adhesion. The contact projections are suitable in particular for the flip-chip technique or for the chip high-speed mounting technique, in which a multiplicity of connections are produced simultaneously by soldering, by

microwelding or by bonding using conductive adhesive or using conductive varnish.

[0024] In one development, the following steps are performed:

[0025] electroplating with a current density in an initial phase, and

[0026] electroplating with a higher current density in comparison with the current density during the initial phase in a main phase following the initial phase.

[0027] This procedure takes account of the lower current-carrying capacity of the basic layer because in the initial phase with a comparatively low current density a layer having a greater electrical conductivity than the basic layer is deposited at the bottom of the openings penetrating through the auxiliary layer. Only when this layer has for example a conductivity corresponding to the thickness of the auxiliary layer (e.g. greater layer thickness), that is to say the auxiliary layer has been "repaired" again with another material, is the current density increased to the high value in order to effect electroplating rapidly.

[0028] In one development, the current density in the initial phase is less than 50 percent of the current density in the main phase. The initial phase is longer than 5 seconds and shorter than 5 minutes. In one refinement, the transition from the initial phase to the main phase takes place with a uniform rise in current over time. In another refinement, the current density is increased multiply in accordance with a stepped sequence, current densities that remain the same in the meantime being used. A superposition of these current density functions with current pulses is also carried out.

[0029] In one development, the current density in the main phase is greater than 0.2 ampere per square decimeter and less than 10 ampere per square decimeter (ASD), e.g. 0.5 A/cm-2. The current density values mentioned relate to the opened resist area on the wafer surface.

[0030] In a next development, the following steps are performed:

[0031] application of an insulating layer prior to the application of the basic layer, and

[0032] patterning of the insulating layer with production of a contact opening prior to the application of the basic layer.

[0033] In the case of a contact projection, the insulating layer is for example a passivation layer which contains for example a silicon oxide layer and/or a silicon nitride layer. The contact opening lies below the mask opening for the electroplating. If the mask opening is chosen to be somewhat wider than the contact opening, then the removal of the residues of the already prepatterned auxiliary layer and of the parts of the basic layer which lie outside the arrangement to be produced is facilitated since the insulating layer is used as an etching stop layer.

[0034] In a next development, the basic layer is a barrier layer against copper diffusion. The auxiliary layer contains copper or comprises copper and is thus particularly well suited to feeding the electroplating current. However, copper is also a material which is particularly corrosive in the presence of moisture, since mixed oxides arise particularly readily, which are also referred to as verdigris. Said mixed oxides considerably reduce the adhesion of the layers in the arrangement to be produced. The current conductivity during operation of the integrated circuit arrangement would thus also be considerably reduced. Since the auxiliary layer is completely removed, in particular in the region in which the layer is electrodeposited or in which the layers are electrodeposited, these disadvantages are not manifested, particularly if the arrangement is also moreover free of copper. In particular, there is also no need for any additional measures for encapsulating copper-containing layers and thus protecting them from moisture.

[0035] In another development, the following steps are performed:

[0036] electroplating of a base layer, and

[0037] electroplating of a covering layer after the electroplating of the base layer, the base layer comprising a different material than the covering layer.

[0038] Consequently, a layer stack is deposited which permits combination effects to be obtained, for example the formation of specific compounds during a subsequent reflow process or the improvement of mechanical properties of the arrangement to be produced.

[0039] In one development, the material of the base layer has a melting point of greater than 500 degrees Celsius and is thus resistant to soldering. The material

of the covering layer has a melting point of less than 400 degrees Celsius and is thus solderable.

The invention additionally relates to a contact projection arrangement, which is also referred to as a soldering bump. The soldering bump contains in the following order with increasing distance from a substrate of an integrated circuit:

[0040] an electrically conductive interconnect for lateral current transport or a connection plate, which is also referred to as a connection pad and serves for vertical current transport, that is to say in a direction exactly opposite to a direction of the normal to a substrate main area,

[0041] an electrically conductive basic layer, in particular an adhesion promoting and barrier layer,

[0042] adjoining the basic layer a copper-free base layer made of a material having a melting point of greater than 500 degrees Celsius, and

[0043] preferably adjoining the base layer an electrically conductive solder material layer having a melting point of less than 400 degrees Celsius.

[0044] The contact projection arrangement according to the invention can be produced particularly well by means of the method according to the invention or one of its developments. In particular, a copper-free contact projection arrangement can be produced using a copper auxiliary layer during electroplating.

[0045] In one development, the base layer contains at least 60 atomic percent of nickel. By way of example, the base layer comprises nickel, nickel-phosphorus or nickel-chromium. Nickel forms a ternary compound with the solder material, e.g. the tin-silver in a boundary layer, the thickness of the boundary layer being limited by self-regulation during the formation of the ternary compounds. Additional measures for defining the thickness of the boundary layer are therefore not necessary. The boundary layer forms an effective barrier against electromigration and, on the other hand, increases the electrical resistance only to a still acceptable extent. The ternary compounds, for example as intermetallic phases, build up a complicated space lattice.

[0046] In one development, the interconnect or the connection plate comprises at least 80 atomic percent of aluminum. As an alternative, however, copper is used as a constituent, with its proportion being more than 50 atomic percent.

[0047] In one development, the basic layer forms a diffusion barrier for copper, so that the copper of the auxiliary layer does not penetrate into the interconnect. In one development, the basic layer comprises titanium-tungsten or contains titanium-tungsten, the proportion of titanium preferably being less than 20 atomic percent. The barrier and adhesion properties of this layer are particularly good. However, other materials are also suitable, such as titanium, tantalum, titanium nitride or tantalum nitride, and layer combinations of these materials are furthermore also possible, e.g. a layer sequence made of a titanium layer, a titanium-tungsten layer and a titanium layer.

[0048] If the basic layer adjoins the interconnect, then no further layers are situated between the basic layer and the interconnect, so that the contact projection arrangement has a simple construction. In particular, no copper-containing layer that would have to be protected against corrosion is situated between the interconnect and the basic layer.

BRIEF DESCRIPTION OF THE DRAWINGS

[0049] The invention is explained below with reference to the accompanying figures, in which:

[0050] Figs. 1A to 1B show production stages during the production of a soldering bump.

[0051] Fig. 2 shows a plan view of the soldering bump after the deposition of a nickel base and prior to the deposition of solder material.

DETAILED DESCRIPTION

[0052] Figs. 1A to 1B show production stages during the production of a soldering bump 10. The method begins proceeding from a substrate 12, which contains for example a plurality of metallization layers (not illustrated) and a main body made of silicon. The metallization layers in each case contain a multiplicity

of interconnects and vias which are insulated by an intralayer dielectric within a metallization layer and by an interlayer dielectric between adjacent metallization layers. A multiplicity of semiconductor components, e.g. field effect transistors of a memory circuit or of a processor, are formed on the main body made of silicon.

[0053] As illustrated in Figure 1A, an upper aluminum layer 14 is applied to the substrate 12 and patterned using a photolithographic method, a connection pad 16 being produced. The aluminum layer 14 and also the connection pad 16 have for example a thickness in the range from 500 nanometers to 2 micrometers, 500 nanometers in the exemplary embodiment. The connection pad 16 has for example a rectangular or square basic area. In the exemplary embodiment, the basic area is octagonal, the distance between two mutually opposite sides of the hexagon being approximately 80 micrometers. The aluminum layer 14 contains only small additions of less than 5 atomic percent, for example 0.5 atomic percent, of silicon, and if appropriate a copper addition, in particular 1 atomic percent.

[0054] After the patterning of the aluminum layer 14, a passivation layer 18 is deposited. The passivation layer 18 has for example a layer thickness in the range from 500 nanometers to 1 micrometer, 500 nanometers in the exemplary embodiment. The passivation layer 18 contains for example an oxide layer and an overlying nitride layer. With the aid of a photolithographic method, a multiplicity of cutouts are introduced into the passivation layer 18 for soldering bumps, one cutout 20 of which is illustrated in Figure 1A. The cutout 20 is for example likewise octagonal, but has a smaller diameter than the connection pad 16. In the exemplary embodiment, the diameter of the cutout 20 is approximately 60 micrometers.

[0055] After the production of the cutout 20, a titanium-tungsten barrier layer 22 is applied over the whole area, the layer thickness of said barrier layer lying e.g. in the range from 100 nanometers to 200 nanometers. In the exemplary embodiment, the barrier layer 22 has a layer thickness of 100 nanometers. The barrier layer 22 contains for example more than 80 atomic percent of tungsten. In the exemplary embodiment, the proportion of tungsten is 90 atomic percent and

the proportion of titanium is 10 atomic percent. The barrier layer 22 is applied by sputtering, for example.

[0056] After the application of the barrier layer 22, a copper layer 24 made of pure copper, e.g. with a proportion of copper of greater than 98 atomic percent, is applied over the whole area. The thickness of the copper layer 24 lies for example in the range from 80 nanometers to 150 nanometers. In the exemplary embodiment, the copper layer 24 has a thickness of 100 nanometers. By way of example, the copper layer 24 is applied by sputtering.

[0057] As is further illustrated in Figure 1A, a resist layer 26, e.g. with a layer thickness of 100 micrometers, is subsequently applied to the copper layer 24. The resist layer 26 is exposed and developed, a cutout 28 arising above the cutout 20. The cutout 28 is likewise octagonal, but has a somewhat larger diameter than the cutout 20. The diameter of the cutout 28 is 80 micrometers in the exemplary embodiment. The cutouts 20 and 28 lie concentrically with respect to one another.

[0058] As is further illustrated by a dashed line 30 in Figure 1A, after the development of the resist layer 26, the copper is removed at the bottom of the cutout 28 by patterning of the copper layer 24 according to the mask formed by the resist layer 26. By way of example, wet-chemical etching is effected, undercuts 32 of the copper layer 32 being noncritical, as will be explained in greater detail below. In another exemplary embodiment, the cutouts are kept small on account of an optimization of the etching and amount to less than 2 micrometers.

[0059] As shown in Figure 1B, a nickel base 50 is subsequently electrodeposited, the copper layer 24 critically serving for carrying current outside the cutout 28. Only at the bottom of the cutout 28 does the barrier layer 20 critically serve for feeding current, in particular at the start of electroplating. By way of example, in accordance with the electroplating method specified above, firstly electroplating is effected only comparatively slowly with a low current density. Once the nickel base 50 has a layer thickness like the copper layer 24, that is to say a layer thickness of 100 nanometers in the exemplary embodiment, a changeover is made gradually or in steps to a higher current density for faster

electroplating. The nickel base 50 is deposited for example with a layer thickness of 2 micrometers to 5 micrometers. In the exemplary embodiment, the layer thickness of the nickel base is 3 micrometers.

[0060] During the deposition of the nickel base 50, the undercuts 32 or these cavities do not cause a disturbance because possible depositions in this region do not adversely affect the functionality of the contact projection.

[0061] As is further shown in Figure 1B, solder material 52 is subsequently electrodeposited, a high current density being used directly at the beginning. In the exemplary embodiment, the solder material is a tin-silver solder deposited with a layer thickness in the range of 50 to 120 micrometers. In the exemplary embodiment, the solder material 52 has a layer thickness of 90 micrometers.

[0062] The electrodepositions of the nickel base 50 and of the soldering material 52 are conformal. An edge 54 of the cutout 20 is mapped as edge 56 on the nickel base 50 and as edge 58 on the solder material 52.

[0063] Figure 1C shows that after the deposition of the solder material 52, the resist layer 26 is removed again, so that the soldering bump 10 is uncovered. The residues of the copper layer 24 are subsequently removed from the barrier layer 22 by wet-chemical or dry-chemical means. Afterward but if appropriate by means of the same etching method, the barrier layer 22 is removed in regions which are not covered by the nickel base 50. A barrier layer region 22a arises between the nickel base 50 and the connection pad 16. The barrier layer region 22a projects beyond the cutout 20 and bears on the passivation layer 18 in the vicinity of the cutout 22a, for example in a vicinity of less than 15 micrometers. Further away from the cutout 20, by contrast, the barrier layer 22 was removed.

[0064] With regard to the removal of the copper layer 24 and of the barrier layer 22, the smallest possible layer thicknesses are chosen for the copper layer 24 and for the barrier layer 22 but without impairing their actual current feeding function and barrier function, respectively, to an excessively great extent.

[0065] The soldering bump 10 is subsequently heated in a reflow step momentarily to a temperature of 400 degrees Celsius, for example, the solder material 52 being reshaped in spherical fashion. A thin boundary layer containing,

inter alia, the ternary alloy tin-nickel-silver forms at the boundary 70 between nickel base and solder material.

[0066] Fig. 2 shows a plan view of the soldering bump 10 after the deposition of the nickel base 50 and prior to the deposition of the solder material 52. The plan view was originally photographed, the resist layer 26 previously having been removed. The octagonal connection pad 16 adjoining for example an interconnect 80 of a rewiring plane is readily discernible. The titanium-tungsten barrier layer 22 is uncovered in the region of the undercuts 32, which have a width B1 of up to 10 micrometers in the circumferential direction.

[0067] The nickel base 50 is delimited by the cutout 28 and has a diameter D of 80 micrometers. The edge 56 of the nickel base 50 is also readily discernible.

[0068] It holds true in summary that the auxiliary layer, in particular the copper layer, is selectively removed in the contact windows, in particular by wet-chemical or galvanic etching-back, which is also referred to as deplating. During galvanic etching-back, the substrate is connected as an anode from which material is removed. The worked-back region is subsequently built again by an electrochemical deposition, e.g. a nickel deposition. Consequently, copper-free interfaces, in particular, are present below the soldering bumps. The following technical effects result:

[0069] [[-]] severe disturbing metallic phase formations, e.g. of copper and tin, no longer occur, and

[0070] [[-]]after resist removal, it is thus possible, under certain circumstances, to remove the UBM (Under Bump Metallization) in a single etching step. This etching is optimized for the removal of the barrier, e.g. titanium or titanium-tungsten. The auxiliary layer and the barrier layer are preferably removed in the same etching chamber, in particular by means of the same etching chemical or etching chemical composition.

[0071] - the undercut of the soldering bump is minimized.

[0072] - for removing the auxiliary layer in the contact windows, it is also possible to use the same electroplating installation as in the case of deposition

within the mask opening, without the substrate being taken from the installation in the meantime,

[0073] [[-]] a plating, for example a nickel plating, directly on to the barrier layer becomes possible.

[0074] A preferred field of application is radio frequency circuits and housings with more than 100 connections which are mounted in accordance with the flip-chip technique. Prior to the electrochemical deposition of solder balls or soldering bumps, a metal barrier, e.g. a titanium layer or a titanium-tungsten layer, and an auxiliary layer, e.g. a copper layer, are applied as a whole-area electrode on the wafer. These two layers may be regarded as UBM (Under Bump Metallization) and are applied for example by magnetron sputtering or electron beam evaporation.

[0075] The barrier layer prevents metallic interdiffusion from the solder material into the interconnects on the wafer. The auxiliary layer serves as a current-carrying contact-making layer for the electroplating process.

[0076] After the lithography, opened resist contact windows are ready for filling with bump metallizations. The electroplating process begins with a wetting or prewetting step for uniformly wetting the contacts with the electrolyte. The first metal layer that is intended to be grown is nickel, for example, e.g. a so-called stud having a thickness of 2 to 5 micrometers or having a thickness in the range of 5 micrometers to 100 micrometers, in particular having a thickness of greater than 40 micrometers. The solder metallization is subsequently deposited with thicknesses of up to 50 micrometers or up to 150 micrometers.

[0077] After resist removal, the barrier layer and the auxiliary layer must be removed again. Wet-chemical methods are employed here. In the course of wet etching, no undesirable undercuts and no corrosion arise as a result of the procedure explained, so that the solder ball still adheres well to the wafer surface.

[0078] Particularly in the case of auxiliary layers made of copper, the formation of severe intermetallic phases of copper with tin and the associated complete dissolution of copper in the tin-silver solder and also the formation of

pores at the interface to the barrier are avoided. A stripping away of the bumps and a failure of the system are effectively prevented.

[0079] It is therefore intended that the foregoing detailed description be regarded as illustrative rather than limiting, and that it be understood that it is the following claims, including all equivalents, that are intended to define the spirit and scope of this invention.